

PB21111710 赵瑞冬 HW1

T3. (1) ALU: 对AB进行运算:

ADD. AND. PASS A. NOT

R2G FILE: 读取 SR1, SR2. 存储/读取 DR

MUX: 数据选择器

MEMORY: 存储单元, 地址+数据

(2) CPU → ALU. MUX

内存 → R2G. MEMORY

(3) 输入: 键盘, mic.

输出: audio. picture.

T4. always @(negedge clk)

begin

if(reset)

begin

q <= 0x12;

end

else

begin

q <= d;

end

end

T2. (1) $(101001)_2 = (29)_{16}$

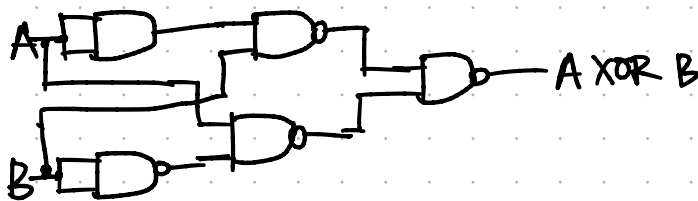
$(52)_8 = (101010)_2 = (2A)_{16}$

$(00101001)_{BCD} = (29)_{10} = (1D)_{16}$

$(33)_{16}$

$\therefore (00101001)_{BCD} < (52)_8$

$< (101001)_2 < (33)_{16}$



USTC

Home

Problem

Status

Welcome, 2202111760

提交结果

1/1 个通过测试用例, 获 10/10 分

状态: Accepted

提交时间: 几秒前

测试用例 0 (行为级仿真): Accepted

10/10 分

Code:

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```
1 module top_module (
2     input clk,
3     input reset, // 异步复位, 高电平有效, 复位值为0
4     output reg [3:0] q);
5     always @(posedge clk or posedge reset)
6     begin
7         if(reset)
8             q <= 0;
9         else
10            q <= q+1;
11        end
12    end
13
14
15 endmodule
```